REMARKS

Claims 1-31 are pending in this application. Claims 18-20 and 25-31 have been subjected to a restriction requirement and have been withdrawn from consideration. Claims 1-6 and 21 have been rejected and claims 7-17 and 22-24 have been allowed.

Rejection – 35 U.S.C. § 102(b) over Nakamura et al.

The Office has rejected claims 1-6 under 35 U.S.C. § 102 (b) as being anticipated by Nakamura et al. (U.S. Patent No. 5,508,534) for the reasons listed on page 2 of the Office Action. Applicant respectfully traverses this rejection.

1. Claim 1 currently recites a method for providing a self-aligned isolation cap on the conductive layer within the trench, where the isolation cap comprises a single layer of a non-organic dielectric material. The Office argues that the method for making the device illustrated in Figure 1 of Nakamura et al. anticipates claim 1.

In Figure 1 of Nakamura et al., the semiconductor device contains a trench gate IGBT where the polysilicon layer 5 in the trench 13 is covered by a CVD oxide film 12, a BPSG film 10, and silicon oxide film 7. *See Figure 1 and column 11, lines 39-59.* Thus, the device of Figure 1 contains two layers of a non-organic dielectric material on the polysilicon layer 5: both a CVD oxide film 12 and a silicon oxide film 7. Accordingly, the Office has not shown that the isolation cap in the device in Figure 1 of Nakamura et al. contains only a single layer of non-organic dielectric material.

2. Claim 3 continues to recite a method containing a step of anisotropically etching the first and second dielectric layers until the upper substrate surface is exposed. The Office argues that the method for making the device illustrated in Figure 1 of Nakamura et al. anticipates claim 3.

Nakamura et al. describe that the device illustrated in Figure 1 is made by providing a trench 13, silicon oxide layer 14, polysilicon layer 5, oxide layer 12, BPSG layer 10, and oxide layer 7. *See Figures 2-6 and accompanying description in columns 11-13.* A resist mask 11 is formed as depicted in Figure 7 and then used to etch layers 7 and 10 to obtain the structure depicted in Figure 8. The etching process uses an aqueous solution containing HF and therefore causes side-etching and produces an undercut in the silicon oxide film 7 shown in Figure 8. *See column 13, lines 50-56.* As recognized by the skilled artisan, such an etching process is an isotropic etching process. Accordingly, the Office has not shown that the method for forming the isolation cap in the device in Figure 1 of Nakamura et al. anisotropically etches the first and second dielectric layers.

3. Claim 6 currently recites a method comprising the step of providing a self-aligned isolation cap on the conductive layer and only within the trench by using a combination of dielectric materials with different etching rates. The Office argues that the method for making the device illustrated in Figure 1 of Nakamura et al. anticipates claim 6.

The device of Figure 1 of Nakamura et al. contains an isolation cap 30 that is formed over the trench 13. *See column 11, lines 56-59.* As depicted in Figure 1, the isolation cap 30 extends outside the trench 13. Accordingly, the Office has not shown that the method of forming the device in Figure 1 of Nakamura et al. forms a self-aligned isolation cap on the conductive layer and only within the trench.

Thus, the Office has not substantiated that Nakamura et al. anticipate every limitation in the rejected claims. Accordingly, Applicants respectfully request withdrawal of this ground of rejection.

Rejection – 35 U.S.C. § 102(b) over Nakamura et al.

The Office has rejected claims 21 under 35 U.S.C. § 102 (b) as being anticipated by Nishihara et al. (U.S. Patent No. 5,541,425) for the reasons listed on page 3 of the Office Action. Applicant respectfully traverses this rejection.

Claim 21 continues to recite a method containing the step of providing a conductive gate on a bottom and sidewall of the gate oxide, where the conductive gate has an upper surface below the upper surface of the substrate. The Office argues that such a claim limitation is described by the method for making the device depicted in Figure 3 of Nishihara et al.

A close examination of Nishihara et al. disproves the Office's argument. The device of Figure 3 contains a trench 13 with an oxide layer 7 formed therein. Next, polysilicon layer 8 (which functions as the gate electrode) is formed on silicon oxide film 7 so as to extend from the inside of trench 13 onto the main surface of the silicon substrate. *See column 10, 33-50.* Since the polysilicon layer extends onto the surface of the substrate, the upper surface of the polysilicon layer 8 is above the upper surface of the substrate. *See also Figures 4-5.*

Thus, the Office has not substantiated that Nishihara et al. anticipate every limitation in the rejected claims. Accordingly, Applicants respectfully request withdrawal of this ground of rejection.

Allowed Subject Matter

Applicant appreciates the indication that claims 7-17 and 22-24 are allowed.

CONCLUSION

For the above reasons, as well as those of record, Applicant respectfully requests the Office to withdraw the pending grounds of rejection and allow the pending claims.

If there is any fee due in connection with the filing of this Amendment, including a fee for any extension of time not accounted for above, please charge the fee to our Deposit Account No. 50-0843.

Respectfully Submitted,

By _____

KENNETH E. HORTON
Reg. No. 39,481

KIRTON & McCONKIE
1800 Eagle Gate Tower
60 East South Temple
Salt Lake City, Utah 84111
Telephone: (801) 328-3600
Facsimile: (801) 321-4893

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